

DOCKET NO.: 4248

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
IN THE MATTER OF THE NEW APPLICATION FOR PATENT

OF: Guenther BERGMANN et al.

USSN: TO BE ASSIGNED

FILED: November 28, 2001

FOR: Method for Tuning a PLL Circuit

USPS EXPRESS MAIL

EL 897 676 822 US

NOVEMBER 28 2001

U. S. PATENT AND TRADEMARK OFFICE
P. O. BOX 2327 (NEW PAT APP)
ARLINGTON, VA 22202

November 28, 2001

FIRST PRELIMINARY AMENDMENT TO MINIMIZE THE FILING FEE

Dear Sir:

In order to minimize the filing fee, please amend the above identified patent application as follows before calculating the filing fee.

In the Claims:

Please cancel claims 8 to 10.


Claims 1 to 7 are maintained for calculating the filing fee.

REMARKS:

After calculating the filing fee, please further enter the accompanying Second Preliminary Amendment which adds new claims 11 to 13 for examination.

Respectfully submitted,
Guenther BERGMANN et al.
Applicant

WFF:ar/4248
Encls.: postcard

By 
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ARLINGTON, VA 22202-0327

November 28, 2001

SECOND VOLUNTARY AMENDMENT

Dear Sir:

After calculating the filing fee and granting a filing date, but before the first examination, please amend the above identified application as follows.

In the Claims:

Claims **1 to 7** are maintained unchanged.

Claims **8 to 10** have previously been cancelled by applicant's First Preliminary Amendment.

Please enter new claims **11 to 13** as follows.

1 **11.** (new) Method according to claim 1, wherein the phase
2 detector (PD) generates a control signal (LD) to indicate
3 that the output frequency (OF) matches the desired
4 frequency (FR).

- 1 **12.** (new) PLL circuit arrangement for implementing the method
2 according to claim 1, comprising
3 a phase detector (PD) which is linked to a loop filter
4 (SF),
5 a voltage-controlled oscillator (VCO) which is wired
6 to the loop filter (SF),
7 at least one control unit (ST) which is linked to the
8 loop filter (SF) and the phase detector (PD) in order to
9 monitor the control voltage (VC) of the oscillator (VCO),
10 and
11 a current source (IQ) and a current sink (IS) which
12 are linked to the loop filter (SF) by means of a switching
13 element (E).
- 1 **13.** (new) PLL circuit arrangement according to claim 12,
2 wherein the control unit (ST) for comparing the control
3 voltage with the two threshold values has at least one
4 comparator and has at least one memory unit for storing the
5 operating state.

REMARKS:

- 1) Before the first examination, please enter the above Voluntary Amendment. No new matter is introduced by the present amendment. New claims 11 to 13 are based directly in sequence on the original literally translated claims 8 to 10 except for omitting the multiple dependencies.

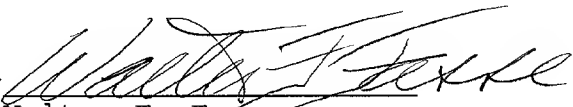
- 2) Examination of the present U. S. application is to proceed on the basis of claims 1 to 7 and 11 to 13. Favorable consideration and allowance of claims 1 to 7 and 11 to 13 are respectfully requested.

Respectfully submitted,

Guenther BERGMANN et al.
Applicant

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